

5/5/2006

PTO/SB/06A (10-01)
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	10/765,301
Filing Date	January 27, 2004
First Named Inventor	Leslie, Terrence
Group Art Unit	2815
Examiner Name	Landau, Matthew

Sheet 1 of 1

Attorney Docket No: 303.860US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
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me		HERGENROTHER, J M., et al., "The vertical replacement-gate (VRG) MOSFET: a 50-nm vertical MOSFET with lithography-independent gate length", <u>Bell Laboratories, Lucent Technologies, Murray Hill</u> , 4pgs (NO DATE) ✓	
me		ISA, "IBM claims speediest silicon transistor", http://www.isa.org/Template.cfm?Section=Communities&template=/TaggedPage/DetailDisplay.cfm&ContentID=20445 , ISA - The Instrumentation, Systems and Automation Society, (November 4, 2002), 2 pgs	
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me		LUCENT TECHNOLOGIES, "Revolutionary transistor turns silicon world on end", (2000), 2 pgs	
me		NING, T H., "Why BICMOS and SOI BiCMoS?", <u>IBM</u> , 0018-8646, (11.29.01), 7 pgs	

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Matthew C. J. [Signature]

DATE CONSIDERED

7/28/06

Substitute Disclosure Statement Form (PTO-1448)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

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PTO/SB/DA(10-01)
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<i>Me</i>		GEPPERT, LINDA, "Triple Gate Double Play: Transistors with three gates and 3-D geometries will replace today's devices in a few years", <u>IEEE Spectrum</u> , (November 2002), 18	

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Matthew C. Fisher

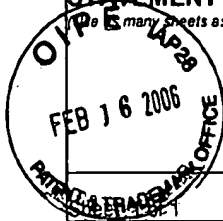
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